Simple Noise Margin Model for Optimal Design of Unipolar Thin-Film Transistor Logic Circuits

Qingyu Cui, Mengwei Si, Radu A. Sporea, and Xiaojun Guo, *Member, IEEE*

***Abstract*— The noise margin (NM) of an inverter is an important feature for the operation stability of the digital circuits. Owing to their simple structure, easy processes, and relatively high gain, the unipolar zero-V_{GS}-load logic design is widely used for implementation of digital circuits in various thin-film transistor (TFT) technologies. In this paper, a simple NM model clarifying the relationship between the NM and electrical/device parameters is developed for the zero-V_{GS}-load inverter. The model is verified by circuit simulations, and is capable of providing a useful guideline for optimal design of unipolar TFT logic circuits. Finally, the application of the derived model in a static random access memory cell design is discussed.**

***Index Terms*— Noise margin (NM), thin-film transistor (TFT), zero-V_{GS} load inverter.**

I. Introduction

With the advances in new semiconductor materials and related processing techniques, thin-film transistors (TFTs) extended their applications from conventional pixel switching to signal processing and interfacing circuits in various large area, flexible, and low cost applications [1]–[6]. However, for TFT technologies in amorphous silicon, organic, and metal oxide semiconductors, it is difficult to find n-type/p-type semiconductor materials with the equivalent performance and compatible processes to build high performance complementary logic circuits. Therefore, various unipolar logic designs are studied for implementation of TFT circuits, including diode-load [7], zero-V_{GS}-load [8], dual-V_{th}, and pseudo-CMOS [9], which are based on p-type TFTs. Among them, the zero-V_{GS}-load logic is popularly used for its circuit simplicity, and relatively high noise margin (NM). The NM of an inverter is an important feature to determine the operation stability of the digital circuits. The influence of the oxide thin-film transistor (OTFT) device parameters, including threshold voltage, device sizing, and supply voltage, on the NM of unipolar TFT circuit design is analyzed in previous work [8]. However, there is still lack of an intuitive analytical model relating the NM to key electrical/device parameters for optimal design. In this paper, a simple NM analytical model is developed for the zero-V_{GS}-load inverter, and is proved to be a useful guideline.

Manuscript received October 15, 2012; accepted February 25, 2013. Date of publication March 21, 2013; date of current version April 18, 2013. This work was supported in part by the National Natural Science Foundation of China under Grant 60906039 and Grant 60910295, the Program for New Century Excellent Talents in University, and the Program for Professor of Special Appointment (Eastern Scholar) at Shanghai Institutions of Higher Learning, and Shanghai Pujiang Program under Grant 11PJ1404700. The work of R. A. Sporea was supported through the Royal Academy of Engineering Academic Research Fellowship Program. The review of this paper was arranged by Editor H. Jaouen.

Q. Cui, M. Si, and X. Guo are with the Electronic Engineering Department, Shanghai Jiao Tong University, Shanghai 200240, China (e-mail: x.guo@sjtu.edu.cn).

R. A. Sporea is with the Advanced Technology Institute, FEPS, University of Surrey, Guildford, Surrey GU2 7XH, U.K. (e-mail: r.a.sporea@surrey.ac.uk).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2013.2251346

II. Derivation of the Model

According to the well-accepted maximum equal criterion (MEC) [8], the NM is defined as the side length of the square, which fits in the inverter transfer curve loops of the maximized area, as shown in Fig. 1. Thus, to obtain the NM value, the initial step is to derive the expression of the inverter's transfer curve.

In the following analysis, the conventional analytical field effect transistor current–voltage model is used, with which, the drain-source current (I_{DS}) in the linear regime is described as

$$I_{DS} = -\left(W/L\right)\mu C_{ox}\left(V_{GS} - V_{th} - V_{DS}/2\right)V_{DS} \quad (1)$$

and in the saturation regime is given by

$$I_{DS} = -\left[W/(2L)\right]\mu C_{ox}\left(V_{GS} - V_{th}\right)^2 \times \left(1 - \lambda\left(V_{DS} - V_{GS} + V_{th}\right)\right) \quad (2)$$

where W is the channel width, L is the channel length, C_{ox} is the dielectric capacitance per area, V_{th} is the threshold voltage, and λ is the output resistance parameter. In the following, for easy derivation of an explicit analytic NM model, λ is taken to be zero, with assuming a large enough output impedance, which is applicable to most of the reported organic and (OTFTs) with relatively long channels. The possible influence of λ will be discussed afterwards.

For the convenience of analysis, as shown in Fig. 1, two critical input voltage (V_{in}) values $V_{in,a}$ and $V_{in,b}$ are defined, to divide the original transfer curve into three regimes for the zero-V_{GS}-load inverter (Fig. 1). $V_{in,a}$ is the input voltage at which the driver TFT transits from the linear regime to the saturation region, whereas $V_{in,b}$ representing the input voltage at which the load TFT transits from the saturation region to the linear regime. Considering the same current passing through the two TFTs, the expressions of the transfer curve in different

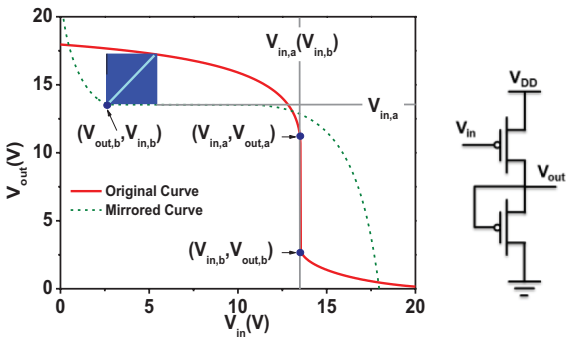

Fig. 1. Illustration of derivation of NM based on MEC for zero-V_{GS}-load inverter.

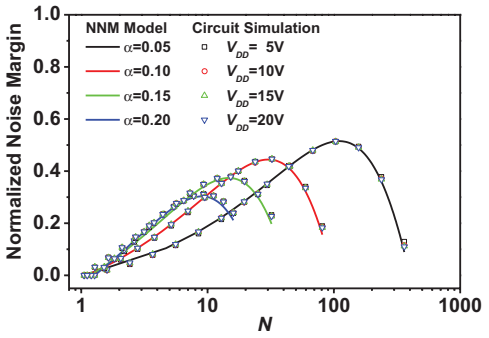

Fig. 2. Verification of developed NNM model by HSPICE circuit simulation with different $\alpha = V_{\rm th}/V_{\rm DD}$ and $V_{\rm DD}$. Initial parameters for each circuit simulation case are derived from $N = (W_L/L_L)/(W_D/L_D)$, α, L, and $V_{\rm DD}$.

regimes can be derived as following:

$$\begin{aligned} &\text{when} \quad V_{\rm in} < V_{{\rm in},a} \\ &\qquad V_{\rm out} = V_{\rm in} - V_{\rm th} \\ &\qquad\qquad +\sqrt{(V_{\rm DD}+V_{\rm th}-V_{\rm in})^2 - N\times V_{\rm th}^2} \qquad (3) \\ &\text{when} \quad V_{\rm in} > V_{{\rm in},b} \\ &\qquad V_{\rm out} = V_{\rm th} \\ &\qquad\qquad -\sqrt{V_{\rm th}^2 - (V_{\rm DD}+V_{\rm th}-V_{\rm in})^2 \big/ N}. \qquad (4) \end{aligned}$$

In the above equations, $N = (W_L/L_L)/(W_D/L_D)$ is the relative sizing of the load TFT to the driver TFT, assuming that all electrical transistor parameters of the driver and the load TFTs are identical $V_{\rm DD}$ is the supply voltage.

In the regime between $V_{{\rm in},a}$ and $V_{{\rm in},b}$, both TFTs are operated in the saturation regime. If considering high output resistance presented in most organic and (OTFTs), $V_{{\rm in},a}$ and $V_{{\rm in},b}$ can be assumed to be of the same value, and the input and corresponding output voltage values can be derived as

$$V_{{\rm in},a} = V_{{\rm in},b} = V_{\rm DD} - \left(\sqrt{N}-1\right) V_{\rm th} \qquad (5)$$

$$V_{{\rm out},a} = V_{\rm DD} - \sqrt{N}\times V_{\rm th}, \quad V_{{\rm out},b} = V_{\rm th}. \qquad (6)$$

With the known expression of the transfer curve, the next step of obtaining the NM value is to decide the left-bottom vertices of the maximum square between original and mirrored transfer curves. On the mirrored transfer curve of the inverter, the point ($V_{{\rm out},b}$, $V_{{\rm in},b}$) is selected as shown in Fig. 1. Then, from this vertex, a straight line is drawn parallel to the line of $y = x$, and the intersection point between this line and the original inverter curve forms the right-top vertex of the NM square. In turn, the NM can be derived as the side length of the square to be expressed by the following equation:

$$\text{NM} = V_{\rm DD} - \sqrt{\left(V_{\rm DD} - \left(\sqrt{N}-1\right)\times V_{\rm th}\right)^2 + N\times V_{\rm th}^2} \qquad (7)$$

where NM is dependent on the electrical parameters $V_{\rm DD}$, $V_{\rm th}$, and N. In practical circuit design, however, inverter circuits could be set with different $V_{\rm DD}$ and it is hard to perform a fair evaluation of the noise immunity capability of various circuit designs. A universal NM criterion independent of the absolute $V_{\rm DD}$ value is therefore preferred. For this purpose, considering that the upper limit of an absolute NM value is $V_{\rm DD}/2$, a normalized NM (NNM) is defined to be $2{\rm NM}/V_{\rm DD}$ and can be derived based on (7) as

$$\text{NNM} = 2\left(1 - \sqrt{\left(1-\left(\sqrt{N}-1\right)\times\alpha\right)^2 + N\times\alpha^2}\right) \qquad (8)$$

where $\alpha = V_{\rm th}/V_{\rm DD}$.

From (8), the NNM depends on two values: 1) the first is N, which represents the sizing information of the zero-$V_{\rm GS}$ load inverter, and 2) the second is $V_{\rm th}$ to $V_{\rm DD}$ ratio α, which represents the electrical information.

III. Model Verification and Discussions

The derived NNM model is verified by comparing the calculated results through the proposed model and those obtained by circuit simulations with HSPICE. In the circuit simulations, the Level-40 HP a-Si TFT model is used [10]. The channel lengths of both TFTs are set to be 10 μm, and the channel width of the driver TFT is 100 μm, whereas that of the load TFT is $100\cdot$N μm. Four α values of 0.05, 0.1, 0.15, and 0.2 applied in the simulations are obtained at different supply voltages ($V_{\rm DD}$) of 5–20 V by choosing corresponding $V_{\rm th}$ values. Other model parameters are set as the default values.

As shown in Fig. 2, the calculated results as a function of N fit well with those obtained by circuit simulations at different α, indicating that the model is effective to describe the relationship of the NM to the device parameter N and the electrical parameter α. Moreover, with the increase of N, the NNM increases in the beginning and starts to decrease after reaching the maximum value. For a given α, the N value for the maximum of NNM, denoted as $N_{\rm opt}$, can be derived from (8)

$$N_{\rm opt} = \left[1/(2\alpha) + 1/2\right]^2. \qquad (9)$$

The maximum of NNM can thus be calculated through

$$\text{NNM}\left(N_{\rm opt}\right) = \sqrt{2}\left(\sqrt{2}-1-\alpha\right) \qquad (10)$$

with the upper limit to be $\sqrt{2}(\sqrt{2}-1) \approx 0.586$. Although a smaller α can help to achieve a higher maximum of NNM, a larger $N_{\rm opt}$ is also required, which may result in layout issues because of the limited layout area. Therefore, the maximum of NNM that can be achieved will be limited by the allowed

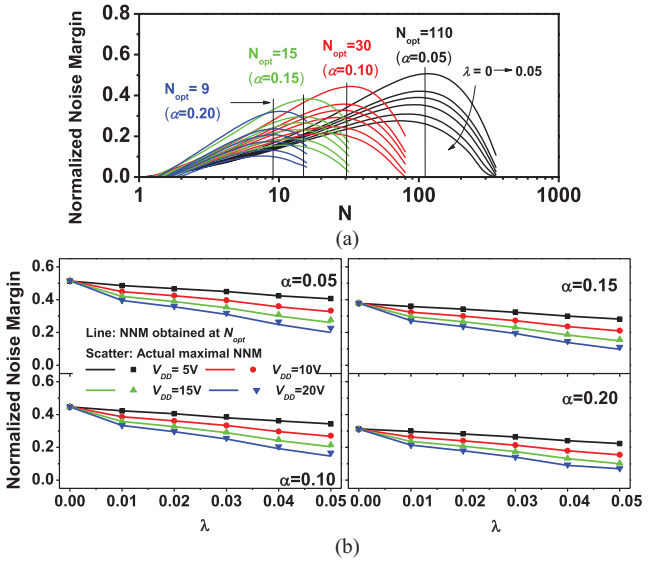

Fig. 3. (a) Curves of NNM as function of N at different λ and α. (b) Comparison of extracted actual maximal NNM values with those obtained at correspondent N_{opt} values derived from (9) at $\lambda = 0$.

largest N value in circuit designs. Eqs. (9) and (10) provide an intuitive guideline of choosing the optimal device sizing to obtain the maximal NM.

If the layout limitation with the allowed largest N value is given, the expression of α value for the maximum of NNM can also be derived from (11) as

$$\alpha_{\text{opt}} = \left[\sqrt{N} - 1\right] \Big/ \left[N + \left(\sqrt{N} - 1\right)^2\right]. \tag{11}$$

Based on (11), the requirements in V_{DD} and V_{th} for the TFTs can be obtained to achieve the highest NM with reasonable layout designs. From Fig. 2, it is generally concluded that α needs to be < 0.2, which means V_{DD} needs to be at least five times greater than V_{th}.

In the above analysis, the output resistance parameter λ of the TFT is taken to be zero by assuming an infinite output resistance. Although an analytical NM equation incorporating the output resistance can also be derived, the form is much more complicated, and cannot show a clear relationship between the NM and the electrical/device parameters for practical use. During the actual circuit design, the main objective is to find the optimal N for achieving the maximized NM. To see whether the derived simple model can be applicable to the case with a finite output resistance ($\lambda > 0$), circuit simulations based on TFT models of different λ in the range of 0–0.05 are performed to obtain the curves of the NNM as a function of N at different λ and α with $V_{\text{DD}} = 15$ V in Fig. 3(a). Based on the curve series, the actual maximal NNM values are then extracted, and compared with those obtained at the correspondent N_{opt} values derived from (9) at $\lambda = 0$, as shown in Fig. 3(b). The NNM values obtained at N_{opt} are quite close to the actual maximal NNM values even when λ is increased to 0.05. Therefore, the derived simplified model is also applicable for the cases of finite output resistance.

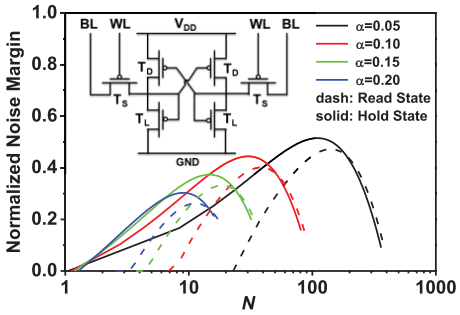

Fig. 4. Calculated NNMs as function N via derived NNM model in read and standby states for SRAM cell based on flip-flop structure composed of two zero-V_{GS} load inverters (inset). Channel width of switch transistor (T_S) is 1/20 that of driver transistor (T_D).

As a practical application example, the derived model is used in predicting the effect of parameter changes on the NM and optimizing the design of a static random access memory (SRAM) cell, which is based on the flip-flop structure composed of two zero-V_{GS} load inverters as shown in the inset of Fig. 4. A SRAM cell should be designed such that under all conditions the NM is reserved to cope with dynamic disturbances. Previously, the derived NM models for analysis and design of SRAMs are based on the CMOS technology [11]. It is very meaningful to investigate how the derived NNM model can be used for the SRAM design in the zero-V_{GS} load logic. The operation of a SRAM could be in three states: 1) read; 2) write; and 3) standby. Considering, the state retention ability is the most important performance of a SRAM, characterized by the NM at the read and standby states, the NNMs at these two states are calculated based on the derived model as a function of N with different α, as shown in Fig. 4. When N is small, the resistance of the load TFT is high, and at the read state, the switch TFT (T_S) draws significant amount current from the main path of the inverter, therefore the NNM at the read state is lower than that of the standby state. As N increases, the resistance of the load TFT T_L is reduced, and the current drawn by T_S becomes ignorable, and thus the NNM of the read state approaches that of the standby state. Based on the results in Fig. 4, the sizing of the TFTs can be determined to achieve the optimized operation stability for the two states. According to above discussions, obviously, the derived NNM model could provide an easy-to-use way for optimizing the design of SRAM cells based on the unipolar TFT technology.

IV. Conclusion

In this paper, a simple normalized model was proposed to build an intuitive relationship between the NM and the key device parameter and design variables for unipolar TFT logic circuits. The model was shown to be in good agreement with circuit simulation results, which proved its accuracy. Based on the model, the upper limit of the zero-V_{GS}-load inverter was derived. The model provided clear guidelines of the device sizing and the ratio of V_{DD} to V_{th} for implementation of high NM logic circuits.

REFERENCES

[1] M. Matsuura, Y. Takafuji, K. Nonomura, F. Funada, and T. Wada, "Liquid-crystal display device with thin-film transistors," in *Proc. SID Symp.*, vol. 23. Jan. 1982, pp. 215–218.

[2] H. Ozaki, T. Kawamura, H. Wakana, T. Yamazoe, and H. Uchiyama, "20-μW operation of an a-IGZO TFT-based RFID chip using purely NMOS 'active' load logic gates with ultra-low-consumption power," in *Proc. Symp. VLSI Circuits*, Jun. 2011, pp. 54–55.

[3] T. Someya, T. Sekitani, M. Takamiya, T. Sakurai, U. Zschieschang, and H. Klauk, "Printed organic transistors: Toward ambient electronics," in *Proc. IEEE Int. Electron Devices Meeting*, Dec. 2009, pp. 1–6.

[4] D. H. Kim, N. Lu, R. Ma, Y. S. Kim, R. H. Kim, S. Wang, J. Wu, S. M. Won, H. Tao, A. Islam, K. J. Yu, T.-I. Kim, R. Chowdhury, M. Ying, L. Xu, M. Li, H.-J. Chung, H. Keum, M. McCormick, P. Liu, Y.-W. Zhang, F. G. Omenetto, Y. Huang, T. Coleman, and J. A. Rogers, "Epidermal electronics," *Science*, vol. 333, no. 6044, pp. 838–843, Aug. 2011.

[5] T. Sekitani and T. Someya, "Human-friendly organic integrated circuits," *Mater. Today*, vol. 14, no. 9, pp. 398–407, Sep. 2011.

[6] T. Sekitani, U. Zschieschang, H. Klauk, and T. Someya, "Flexible organic transistors and circuits with extreme bending stability," *Nature Mater.*, vol. 9, pp. 1015–1022, Nov. 2010.

[7] K. Myny, M. J. Beenhakkers, N. A. J. M. Van Aerle, G. H. Gelinck, J. Genoe, W. Dehaene, and P. Heremans, "Unipolar organic transistor circuits made robust by dual-gate technology," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1223–1230, May 2011.

[8] S. De Vusser, J. Genoe, and P. Heremans, "Influence of transistor parameters on the noise margin of organic digital circuits," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 601–610, Apr. 2006.

[9] T. C. Huang, K. Fukuda, C. M. Lo, Y. H. Yeh, T. Sekitani, T. Someya, and K. T. Cheng, "Pseudo-CMOS: A design style for low-cost and robust flexible electronics," *IEEE Trans. Electron Devices*, vol. 58, no. 1, pp. 141–150, Jan. 2011.

[10] *HSPICE MOSFET Models Manual*, Synopsys, Mountain View, CA, USA, 2007.

[11] E. Seevinck, F. J. List, and J. Lohstroh, "Static-noise margin analysis of MOS SRAM cells," *IEEE J. Solid-State Circuits*, vol. 22, no. 5, pp. 748–754, Oct. 1987.

Authors' biographies and photographs not available at the time of publication.